IN THE CLAIMS

1. (Original) A system for providing parallel processing of data to a plurality of digital signal processors (DSPs), comprising:

means for transmitting communication data to a load management system from a CPU;

means for selecting a digital signal processor (DSP) from a plurality of DSPs for processing the communication data;

means for processing the communication data using the selected DSP; and

means for transmitting the processed data back to the CPU and to a communication device.

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2. (Original) A system of claim 1, wherein the communication data is transmitted from a VoIP medium.

3. (Original) A system of claim 1, wherein the communication data is transmitted from a FoP medium.

4. (Original) A system of claim 1, wherein the communication data is transmitted from an IP to sonet medium.

5. (Original) A system of claim 1, wherein the communication data is transmitted from an encoder/decoder.

6. (Original) A system of claim 1, wherein the communication data is transmitted from a broadband communication medium.

7. (Original) A system of claim 1, wherein the communication data is transmitted from an image processing medium.

8. (Original) A system of claim 1, wherein the communication data is transmitted from a data modem.

9. (Original) A system of claim 1, wherein the load management system comprises:

a plurality of direct memory access (DMA) devices having internal registers, a plurality of FIFOs, a plurality of state machines associated with the plurality of FIFOs, and a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and controls registers coupled to the plurality of DMA devices;

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a CPU interface for interfacing the CPU with the plurality of status and control registers; and

a DSP interface for interfacing the plurality of DSPs with the plurality of DMA devices.

10. (Original) A system of claim 9, wherein the DSP interface includes a program/data memory and a ping pong memory.

11. (Original) A system of claim 9 further comprising an external memory, wherein the external memory is coupled to the plurality of DSPs through dedicated memory threads.

12. (Original) A system of claim 9, wherein the CPU interface includes a routing MUX, wherein the routing MUX is coupled to the external memory device.

13. (Original) A system of claim 12, wherein the external memory device comprises a memory access controller array.

14. (Original) A system of claim 12, wherein the external memory device comprises a memory management system.

15.-32. (Cancelled).